Trends in CMOS Image Sensor Technology and Design

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Abstract

Three trends that promise to increase CMOS image sensor system performance are presented: (i) modifications of deep submicron CMOS processes to improve their imaging characteristics, (ii) developments that take advantage of these modified deep submicron processes, and (iii) high frame rate sensors and applications to still and video imaging, specifically to extending sensor dynamic range. Recent research on Digital Pixel Sensors and applications of its high frame rate to still and video imaging are discussed.

Introduction

CMOS image sensors have received much attention over the last decade, offering the promise of ultra low power and camera-on-chip integration. Recently, they have transitioned from research prototypes to high volume production with over 30 million sensors shipped this year and an estimated annual growth rate of over 40% (In-Stat/ MDR August 2002). Most CMOS sensors shipped today are application-specific, *e.g.*, for optical mouse, or used in low-end applications, *e.g.*, PC-cameras and toys. Fabricated in older CMOS technologies (0.35μm and above), these sensors generally have large pixels, low resolutions (VGA and below), and moderate integration. With few exceptions [1], they have lower performance than CCDs and as a result are not used in digital cameras. Recent technology and design developments in several areas including silicon processing, color filter array and microlens integration, package miniaturization [2], and pixel and camera-on-chip design, promise to broaden the applicability of CMOS image sensors, and to enhance their performance and functionality even beyond that of CCDs.

In this paper we discuss three interrelated developments focused on enhancing CMOS image sensor system performance: (i) modifications of deep submicron CMOS processes to improve their imaging characteristics, (ii) developments that will take advantage of the modified deep submicron processes, and (iii) high frame rate sensors and applications to still and video imaging, specifically to extending sensor high dynamic range beyond that of CCDs. We briefly describe our group's recent work in the later two areas.

Technology Modifications

CMOS image sensors benefit from technology scaling by reducing pixel size, increasing resolution, and integrating more analog and digital circuits on the same chip with the sensor. At 0.25μm and below however, a digital CMOS technology is not directly suitable for building high quality image sensors. The use of shallow junction and high doping result in low photoresponsivity, and the use of shallow trench isolation (STI), thin gate oxide, and salicide cause high dark current. Furthermore, in-pixel transistor leakage becomes a significant source of dark current. Indeed in a standard process, dark current due to reset transistor off-current and the follower transistor gate leakage current in an Active Pixel Sensor (APS) [3] pixel can be orders of magnitude higher than the diode leakage itself. As a result of these major problems, process modifications are mandatory.

Recent papers have reported on several modifications to standard CMOS technologies to improve their imaging performance, *e.g.*, [4]. To increase photoresponsivity, non-silicided deep junction diodes (NW/PSUB or Ndiff/PSUB) and integrated microlens arrays are used. The doping profiles of these diodes are optimized to increase quantum efficiency at visible wavelengths and to lower capacitance. Different SiON materials are being tried out to increase light transmission. To reduce dark current non-silicided, double-diffused source/drain implantation is used. Hydrogen annealing was also shown to reduce leakage by passivating defects [4]. The use of pinned photodiodes [1] also significantly reduces dark current due to the quenching of surface-interface traps by an implanted p-region, while providing more complete resets, thereby reducing reset noise and lag. To reduce transistor leakage, both the reset and follower transistors in an APS are fabricated with thick gate oxide (70Å). The thresholds of these two transistors are also adjusted to further reduce leakage and increase voltage swing. The reset transistor threshold is increased to reduce its off-current, while the follower transistor threshold is decreased to improve

voltage swing. With these process modifications, image sensors implemented in 0.18μm CMOS technology can achieve high QE and low dark current of sub-1 nA/cm^2 [4].

Triple-Well Photodetector

Color imaging today is implemented by depositing photoresist color filter arrays (CFA) in a mosaic pattern on top of the sensor array. This approach has several shortcomings including reduced spatial resolution, color crosstalk, and increased distance from the microlens to the photodetector. Foveon's triple-well diode approach [5] promises to increase spatial resolution and reduce spatial color crosstalk of conventional CFAs by having each pixel output three colors. It exploits the dependency of the absorption coefficient on wavelength, whereby longer wavelengths are absorbed at greater depths. As shown in Figure 1, a triple well photodiode structure with three separate readout ports is employed. The output from the shallowest junction corresponds to Blue, the middle junction to Green, and the deepest junction to Red. Although this approach eliminates the need for a CFA and demosaicing, thus improving spatial resolution, it has two shortcomings: (i) larger pixel size than conventional APS (which would mean small number of pixels for the same sensor area), and (ii) high correlation between the three channels. Figure 2 plots the relative color spectral responses for a sensor using standard RGB CFA and the Foveon sensor. Note that the overlap between the channels is higher for the Foveon sensor.

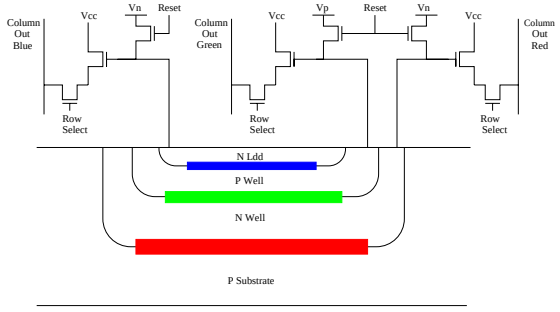


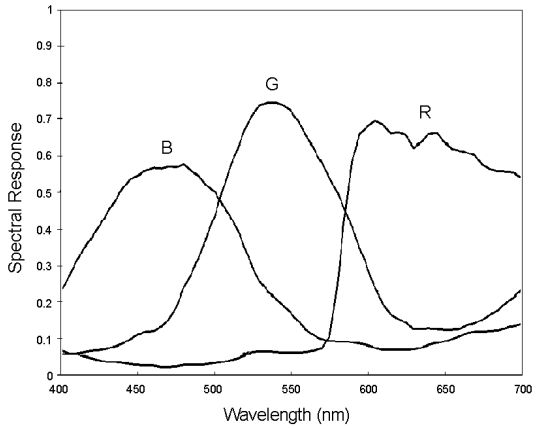
Fig. 1. Triple-well pixel.

Design Trends

A direct application of the modified 0.25μm and below CMOS technologies is the design of very high resolution sensors. In [6], it is pointed out that the memory-like architecture of CMOS image sensors make them better suited for multi-mega pixel resolutions than CCDs, whose readout is intrinsically serial.

Perhaps the most far reaching advantage of CMOS

Source: TSMC



Source: Dick Lyon, Foveon

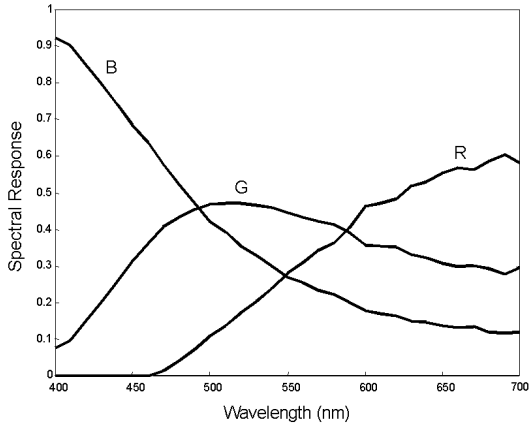


Fig. 2. RGB spectral response for (top) standard CFA and (bottom) Foveon sensor.

image sensors over CCDs is the ability to integrate analog and digital processing on the same chip with the sensor. All CMOS image sensors today include circuits for signal conditioning, readout, sequencing and clock distribution, some integrate ADC, and a few integrate signal processing circuits for color processing or for non-imaging applications. As CMOS image sensor technologies scale it will become possible to integrate all basic camera functions on chip, *e.g.*, [7], to enable applications requiring very small form-factor and ultra-low power consumption. Integration will also enable the development of more advanced application-specific devices, *e.g.*, for 3D imaging [8] and biometrics.

Another trend that takes advantage of scaling is increasing pixel-level processing by adding more transistors to each pixel. As an example, the Stanford Programmable Digital Camera (PDC) group has been exploring image sensor architectures with per-pixel ADCs. These architectures, referred to as Digital Pixel Sensor (DPS) [9], offer several advantages over current analog pixel architectures such as APS

including, better technology scaling due to reduced analog circuit performance demands, the elimination of column temporal noise and FPN, and high speed readout. The group has developed three generations of DPS architectures. The most recent [9] is a 352×288 pixel sensor with per-pixel, 8 bit-parallel single-slope ADC operating at a continuous rate of 10,000 frames/s (1 Gpixel/s), fabricated in a standard 0.18μm CMOS technology. Each pixel consists of an nMOS photogate, a transfer gate, reset transistor, a storage capacitor, a 1-bit comparator, and 8 3T memory cells in an area of $9.4\mu\text{m} \times 9.4\mu\text{m}$ (see Figure 3). The photogate subcircuit uses thick oxide (3.3V) transistors (labeled * in the figure) to combat the high gate and subthreshold leakage currents and the low supply voltage problems of the 1.8V thin oxide transistors.

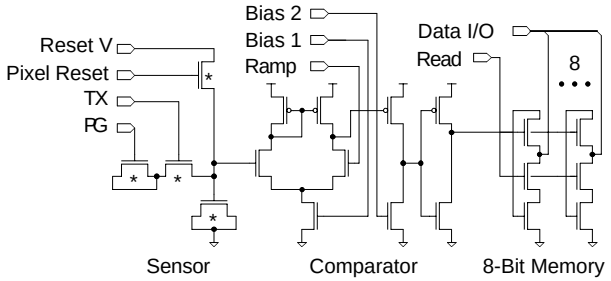


Fig. 3. DPS pixel schematic.

Taking advantage of CMOS scaling, a recent paper [10] has investigated using metal patterns deposited on top of a photodetector in place of CFAs. It was demonstrated that wavelength selectivity can be controlled by varying the spacing and number of layers of the metal patterns above each pixel's photodetector. Using 0.13μm or below technology or multiple patterned metal layers in 0.18μm, good selectivity in the visible range can be achieved.

High Frame Rate Sensors and Applications

Several recent papers have reported on CMOS image sensors operating at over 500 frames/s, *e.g.*, [11], [9]. In addition to high speed imaging applications, several researchers have recently shown that high frame rate can also benefit still and video rate imaging [12], [13]. The idea is to use the high frame rate to oversample the scene thus obtaining more accurate information about illumination and motion. This information can then be used to: (i) enhance image quality, (ii) improve the performance of video applications, or (iii) simplify many low-level vision algorithms, *e.g.*, feature tracking.

An important application that the PDC group has

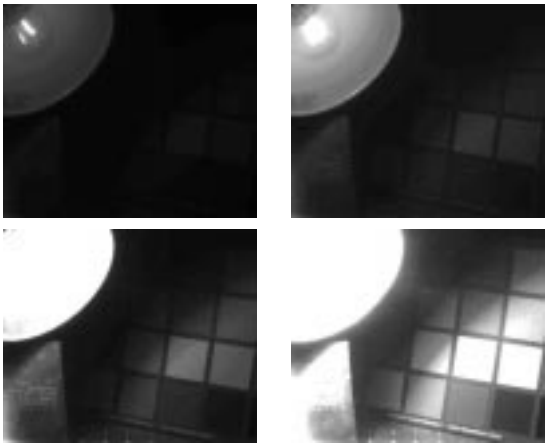


Fig. 4. Four of the 500 non-destructively captured images, each with increasing exposure time.

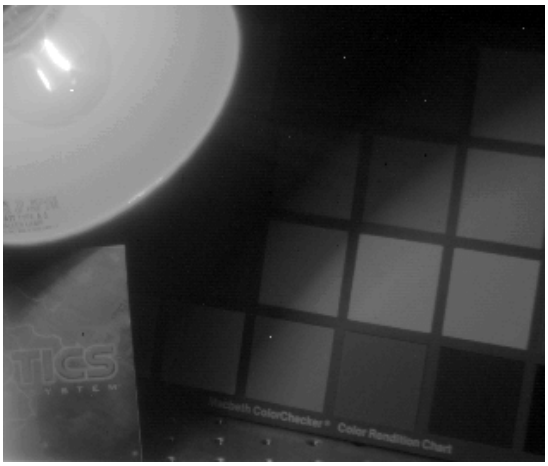


Fig. 5. Synthesized high dynamic range image.

been investigating is sensor dynamic range extension using multiple capture (see Figure 4). Using the latest DPS chip 500 images of a high dynamic range scene were non-destructively captured at a rate of 1400 frames/s. Note that no single image captures both the dark and bright regions of the scene. The high dynamic range image rendered in Figure 5 was synthesized from the 500 images by simply using an appropriately scaled version of the last sample before saturation for each pixel [14].

Although other techniques have been proposed for extending sensor dynamic range, *e.g.*, well capacity adjusting [15] and time-to-saturation [16], only multiple capture has been shown to extend dynamic range at the low illumination end. In [14], an algorithm for reducing read noise by weighted averaging of each pixel's samples before saturation was proposed. Figure 6 illustrates the gain in SNR and DR obtained using this algorithm. We also investigated two other applications of high frame rate, motion blur prevention

[14] and accurate optical flow estimation [13]. Such accurate optical flow estimates can be used as a basis for implementing many video applications, including compression, motion tracking, super-resolution and most recently sensor gain FPN correction [17].

The implementation of these high frame rate applications, however, requires very high bandwidth between the sensor, the memory and the processors making a multi-chip implementation impractical. In [13] we argue that integrating embedded DRAM and digital signal processing with a high speed readout CMOS image sensor such as DPS on a single chip in 0.18μm CMOS technology and below can enable cost effective implementations of several still and video imaging applications.

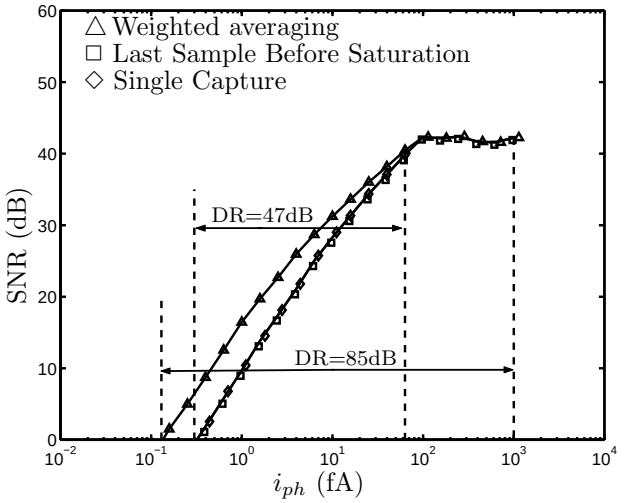


Fig. 6. DR and SNR with and without read noise reduction.

Conclusion

Three trends in CMOS image sensor technology and design are discussed. First we presented several modifications that have been shown to enhance deep submicron CMOS technology imaging performance. We showed that such modified processes will enable (i) multi-mega pixel sensors, (ii) camera-on-chip integration, (iii) per-pixel ADC, (iv) integration of embedded DRAM and processing with a sensor to exploit the high frame rate capability of the sensor, and (iv) wavelength selectivity via metal patterns. Finally we discussed high frame rate applications to still and video rate imaging, in particular, dynamic range extension via multiple capture. These trends, we believe, will ultimately enhance CMOS image sensor performance beyond that of CCDs.

Acknowledgment

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