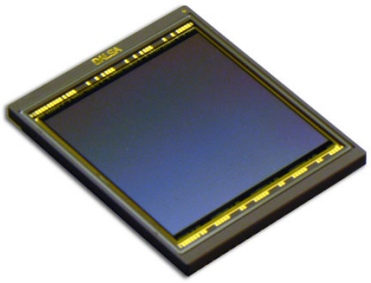
DALSA IA-DJ High Quanta

Imaging Sensor

Features

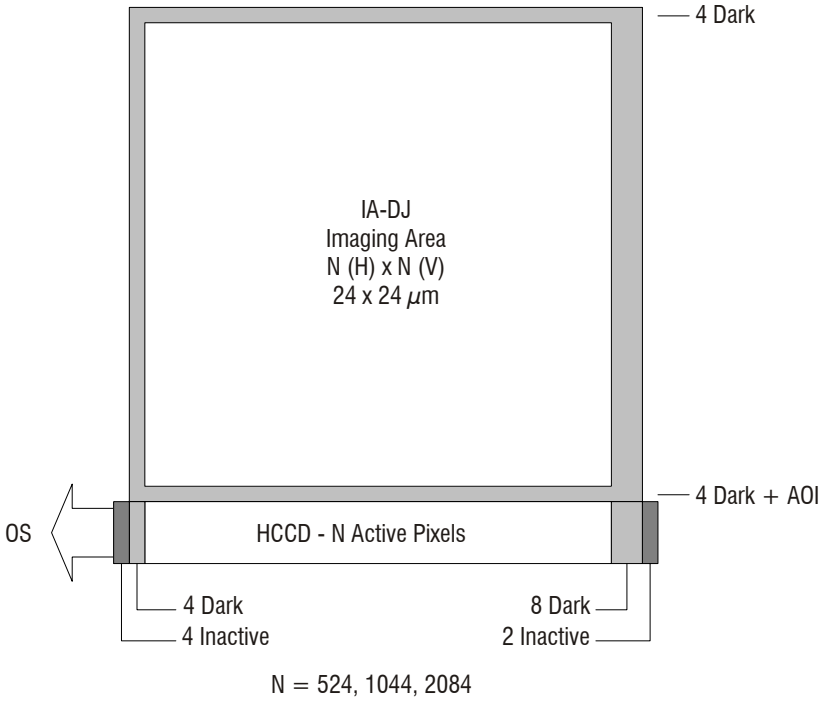


Front illuminated full-frame CCD
High QE response
24 μm × 24 μm pixel size
524×524, 1044×1044, or 2084×2084 pixel resolution
Low dark current (< 15 pA/cm^2 @ 25 °C)
Dark signal noise <1 e- / pixel per second at -16 °C
Single output, up to 10 MHz data rate
1×1, 2×2, or 4×4 binning modes
High speed Area of Interest (AOI) mode
~100% fill factor (approx.)
Photo-sensitive readout registers for real-time exposure monitoring

Description

The IA-DJ High Quanta full-frame CCD sensors are designed to meet the requirements of scientific and x-ray applications demanding high sensitivity, high frame rates and low noise performance. The High Quanta series of sensors aims to provide the highest quantum efficiency in a front-illuminated sensor.

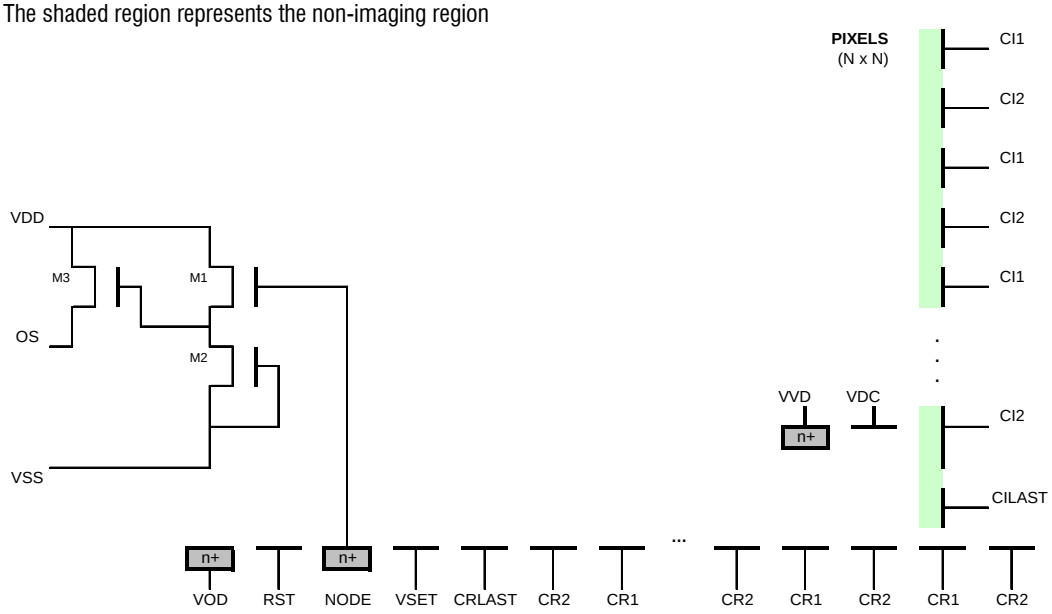
Sensor Block Diagram



3-Sep-09
03-036-20007-01
www.dalsa.com

Gate Structure Diagram

The shaded region represents the non-imaging region



Functional Description

The IA-DJ sensors are composed of three main functional groups: photo pixels, in which the charge packets are generated, CCD readout shift registers, and output amplifiers where the charge packets are converted to voltage pulses.

Detection

The IA-DJ sensors are available in 524 × 524, 1044 × 1044, 2084 × 2084 pixel resolutions. The pixels are 24 × 24 μm in size. Light incident on these pixels is converted into charge packets whose size (i.e. the number of electrons) is linearly dependent upon the light intensity and integration time.

Transfer

The pixels act as true two-phase CCD buried channel shift registers to transfer the charge packets vertically. These vertical registers clocks (Clx) control the transfer of charge into the CR1 of the horizontal two phase CCD shift register. There are isolation CCD pixels at the end of the horizontal shift register which must be considered when clocking the sensor. Please refer to sensor functional diagram for details.

Output

The signal charge packets are transferred serially from the horizontal shift registers, over the SET gate (VSET bias), and to the floating sense diffusion. As the charge is received, the corresponding potential on the diffusion is applied to the input of a low noise, high sensitivity amplifier, producing an output signal voltage on OS. The floating sense diffusion is cleared of signal charge by the reset gate (RST) to a voltage level equal to the potential on the output drain diffusion (VOD) in preparation for the subsequent signal charge packet. AC coupling to the output is recommended to eliminate the DC offset.

Sensor Architecture

Image Section	IA-DJ-00524	IA-DJ-01044	IA-DJ-02084
Active Image	12.58 × 12.58 mm	25.06 × 25.06 mm	50.02 × 50.02 mm
Aspect Ratio	1:1	1:1	1:1
Pixel width × height	24 × 24 μm	24 × 24 μm	24 × 24 μm
Pixel Optical Fill Factor	97.5 %	97.5 %	97.5 %
Number of active lines	524	1044	2084
Number of dark lines	8	8	8
Total number of lines	532	1052	2092
No. of active pixels per line	524	1044	2084
No. of dark + inactive pixels per line	18	18	18
Total No. of pixels per line	542	1062	2102

Output Section	
Output Amplifier	2 stage source follower
No. Output	1
Amplifier Load Current	External

Sensor Pinout

Signal Name	Signal Description
CI1	Vertical CCD Clock - Phase 1
CI2	Vertical CCD Clock - Phase 2
CILAST	Last Vertical CCD
VBB	Substrate
VGR	Guard Ring
VVD	AOI Drain
VDC	AOI Gate
CR1	Horizontal CCD – Phase 1
CR2	Horizontal CCD – Phase 2
CRLAST	Last Horizontal CCD
VSET	Output node Set Gate
RST	Reset Gate
VSS	Amplifier Return
VOD	Reset Drain
VDD	Amplifier Supply
OS	Video Output

Notes:

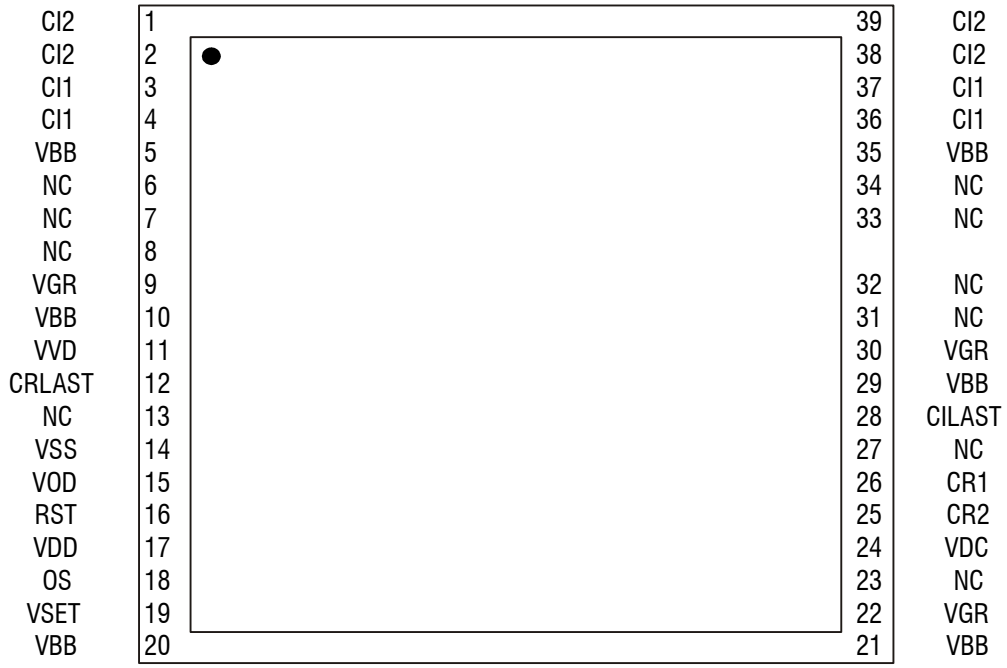
1. All CI1 pins must be connected together – only one Phase 1 clock driver required
2. All CI2 pins must be connected together – only one Phase 2 clock driver required
3. All VBB pins should be connected together to GND
4. All VGR pins should be connected together to a common potential

Power Sequencing

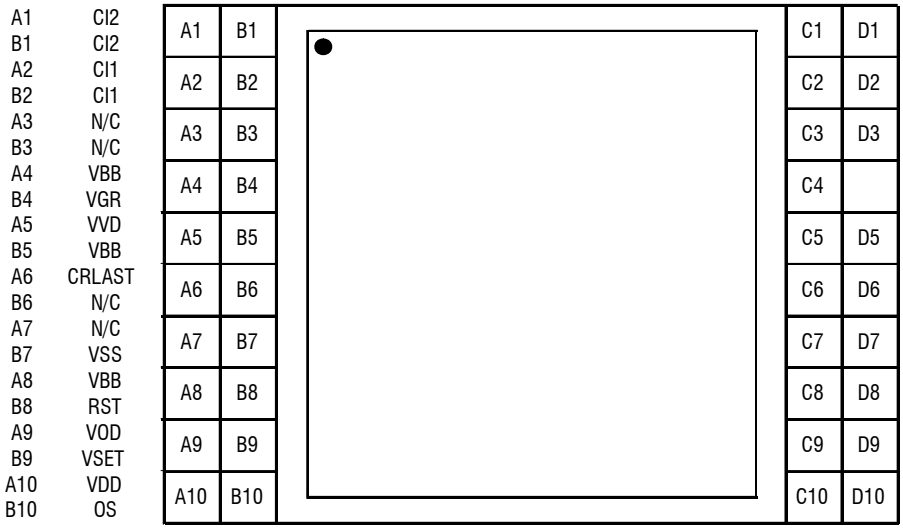
Power On	
1	VBB
2	VSS
3	VOD
4	RST
5	Rest of biases

POWER OFF: Reverse sequence of POWER ON.

IA-DJ-2084 Pinout Drawing



IA-DJ-00524 and IA-DJ-01044 Pinout Drawing



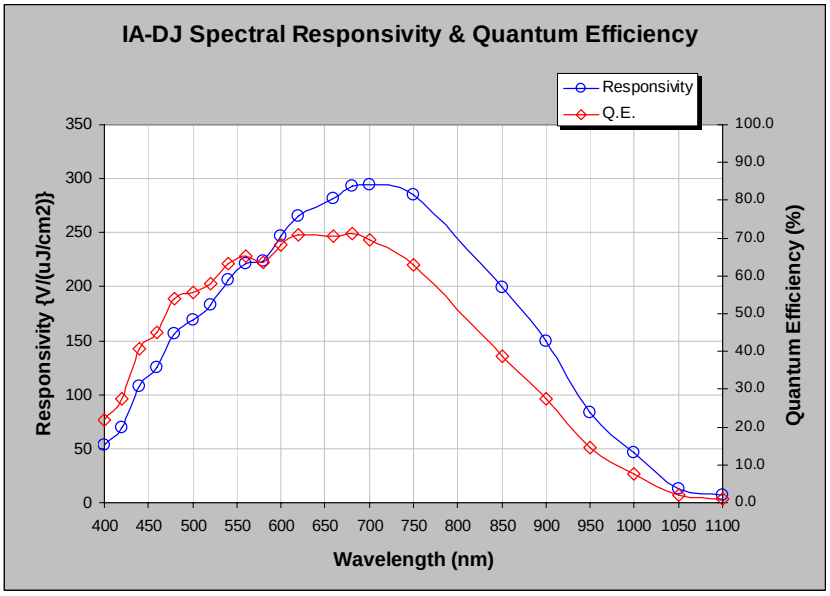
Additional Performance Specifications

Parameter	Minimum	Typical	Maximum
Full Well Capacity[1] ($N_{e\text{-}sat}$)	150 Ke^-	170 Ke^-	200[1] Ke^-
Charge Conversion Efficiency (CCE)	20 $\mu V/e^-$	21.0 $\mu V/e^-$	21.5 $\mu V/e^-$
RMS noise[2]	-	13 e^- rms	20 e^- rms
Dynamic range[3]	81 dB	82 dB	-
Charge Transfer Efficiency (CTE)	0.99999	>0.99999	-
Dark current density[4] (J_d)	-	13 pA/cm^2	15 pA/cm^2
	-	470 e^-pixel/sec	540 e^-pixel/sec
Dark current doubling temp	5 °C	5.5 °C	6 °C
Wavelength at peak responsivity	660 nm	680 nm	-
Peak responsivity	280 V/(μJ/cm^2)	290 V/(μJ/cm^2)	295 V/(μJ/cm^2)
QE	-	See the responsivity graph	-
OS Linearity[5]	-	<1 %	-
Anti-blooming	-	none	-

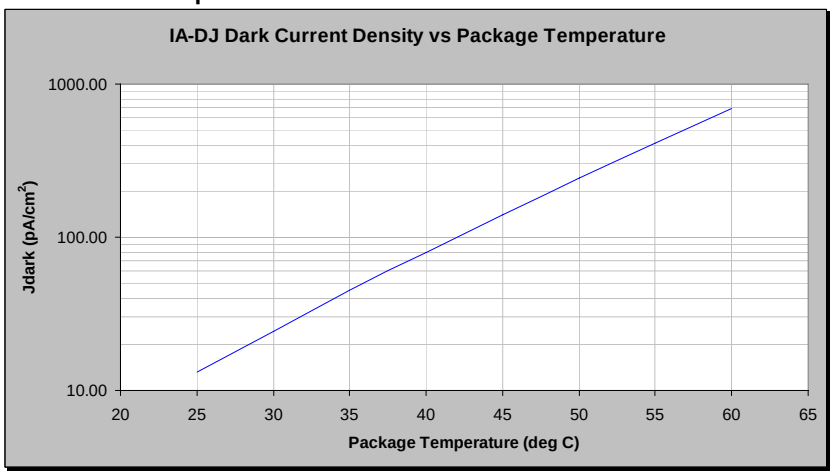
Notes:
1. VOD and RST DC biases can be adjusted to increase the $N_{e\text{-}sat.}$ OS linearity may suffer near 200 Ke^- $N_{e\text{-}sat}$.
2. Noise floor of the CCD Amplifier assuming correlated double sampling, data rate = 5 MHz, temperature = -20°C, bandwidth = 17 MHz.
3. 20LOG($N_{e\text{-}sat}$/RMS Noise) using typical rms noise (see note 2).
4. At 25°C – see the dark current graph, below.
5. Worst case deviation from best fit line defined by 10% to 95% of VSAT.

Operating Conditions:
1. All values are measured using typical operating conditions
2. Ambient Temperature = 25°C
3. f_{DATA} = 5MHz (no binning)
4. I_{LOAD} = 3 mA
5. Tungsten halogen light source, black body color temperature 3200k, filtered with 750 nm IR cutoff filter. (except QE measurement)

Responsivity and QE Graph



Dark Current Graph



Cosmetic Specification

IA-DJ-00524

Grade	Point Defect	Clusters I ≤ 5	Clusters II ≤ 10	Clusters III ≤ 20	Column Defect	Double Column
Class I	≤ 5	≤ 2	0	0	0	0
Class II	TBD	TBD	TBD	TBD	TBD	TBD

IA-DJ-01044

Grade	Point Defect	Clusters I ≤ 5	Clusters II ≤ 10	Clusters III ≤ 20	Column Defect	Double Column
Class I	≤ 15	≤ 5	0	0	0	0
Class II	≤ 40	≤ 10	0	0	≤ 2	0

IA-DJ-02084

Grade	Point Defect	Clusters I ≤ 5	Clusters II ≤ 10	Clusters III ≤ 20	Column Defect	Double Column
Class I	≤ 50	≤ 10	0	0	0	0
Class II	≤ 100	≤ 20	≤ 5	≤ 5	≤ 4	0

Test Grade Sensors
Test grade sensors may be available, by request. Test grade sensors are functional sensors provided for engineering development purposes only. These sensors have an unspecified number of cosmetic defects and may not meet all sensor specifications. Not all parameters may be tested.

Defect Description

General:

- An exclusion zone consisting of the outside two rows and columns on all sides are excluded from defect calculations
- Specification apply at 25°C ambient
- Deviations are calculated with respect to the frame mean, which does not include the exclusion zone and any column defects

Point Defect:

- Under Light
  - A pixel which deviates by more than ±20% from neighboring pixels when illuminated to 70% of saturation.
- Under Dark
  - A pixel whose dark current exceeds 4500 electrons/pixel/second at 25°C.

Cluster Defect:

- A grouping of adjacent single pixel defects
- Pixel defects are defined as adjacent if they share a common side or a common corner
- Cluster defects are separated by at least 2 pixels from other cluster defects

Column Defect:

- A grouping of more than 10 single pixel defects along a single column
- A column that does not exhibit the minimum charge capacity specification (Low charge capacity)
- A column that loses >500 electrons when the array is illuminated to a signal level of 2000 electrons/pix. (Trap like defect)
- Column defects are separated by at least 5 pixels from other column defects

Operation

Absolute Maximum Rating	Min	Max
Storage Temp	-20 °C	80 °C
Operating Temp	-20 °C	60 °C
Voltage on CI1, CI2, CILAST, VDC, CR1, CR2 with respect to VBB	-10 V	18 V
Voltage on OS, VDD, VOD, VSS, VVD, VGR, RST, VSET, CRLAST	0 V	18 V
Amplifier Load Current (I_{LOAD})		8 mA

Note:

1. A special package is required for operation down to -60 °C. Please contact your local DALSA representative for more information.

Input/Output Characteristics

Input Characteristics: Capacitance to VBB	Units	IA-DJ-00524	IA-DJ-01044	IA-DJ-02084
From CI1, CI2[1]	pF	N/A	N/A	148000
From CILAST	pF	N/A	N/A	81
From CR1, CR2[2]	pF	N/A	N/A	390
From CRLAST	pF	N/A	N/A	20
From RST	pF	N/A	N/A	25
From VDC	pF	N/A	N/A	65
Output Characteristics:				
Output Impedance (R_{OUT})[3]	Ω	700	700	700
DC Output Offset (VOS)[3]	V	11.8	11.8	11.8

Notes:

1. Contribution from each CI pin. CI1 pins 3, 4, 36, 37 are internally connected. CI2 pins 1, 2, 38, 39 are internally connected.
2. Contribution from each CR pin.
3. I_{LOAD} = 3 mA

DC Operating Conditions

Symbol	Description	Unit	Min.	Rec.	Max
I_{LOAD}	Load current to the output (OS)	mA	2.0	3.0	5.0
VDD	Amplifier Supply	V	16.5	17.0	17.5
VOD	Output reset drain	V	15.0	15.5	16.0
VSET	Output node set gate	V	1.0	2.0	2.0
VVD	AOI Drain	V	10.0	12.0	14.0
VSS[1]	Amplifier Return	V	2.0	2.0	2.5
VBB[1]	Substrate	V	0	0	0
VGR	Guard Ring	V	9.0	10.0	14.0

Note:
1. VBB should never be forward biased with respect to VSS. To protect against damage, a Schottky diode between VBB and VSS is recommended

AC Operating Conditions

Symbol	Description		Unit	Min.	Rec.	Max
Clx	All Clx Clocks (VCCD)	low*	V	-8.5	-8.0	-7.8
		swing*	V	10.5	11.0	12.0
CRx	All CRx Clocks (HCCD)	low	V	0	0	0
		swing	V	4.8	5.0	6.5
RST[1]	Reset Clock	low	V	2.0	2.5	3.3
		swing	V	8.5	9	11
VDC	AOI Pixel Reset Clock	low	V	-8.5	8.0	-7.8
		swing	V	11.0	12.0	13.0
f_{DATA}	Data rate		MHz	1.0	5.0	10.0

Note:

1. RST pulse FWHM should be at least 20ns.

IA-DJ-00524 Frame Rate

Binning Mode	Data Rate (MHz)	CR Clock[1] (MHz)	f_{FRAME}[2] (Hz)
No binning	5	5	14.1
2 × 2	5	10	43.3
4 × 4	5	20*	95.6

IA-DJ-01044 Frame Rate

Binning Mode	Data Rate (MHz)	CR Clock[1] (MHz)	f_{FRAME}[2] (Hz)
No binning	5	5	4.0
2 × 2	5	10	13.7
4 × 4	5	20*	36.3

IA-DJ-02084 Frame Rate

Binning Mode	Data Rate (MHz)	CR Clock[1] (MHz)	f_{FRAME}[2] (Hz)
No binning	5	5	1.0
2 × 2	5	10	3.9
4 × 4	5	20*	12.2

Notes:
1. CRLAST needs to be maintained at Data Rate for proper binning.
2. Zero integration time, max frame rate. Overclock pixel = 20.
3. This is the maximum allowed HCCD clock rate.

Timing Parameters

Symbol	Description	Unit	Min.	Rec.	Max.
t_1	CI1 duration	ns	-	$2t_2 + t_3$	-
t_2	CI2 duration	ns	4000	5000	-
t_3	CI1/CI2 overlap	ns	100	500	-
t_4	HCCD setup time	ns	$0.5t_2$	t_2	-
t_5	HCCD period (no binning)	ns	-	200	-
t_6	RST pulse duration (FWHM)[2]	ns	15	20	$0.25t_5$
t_7	Overclock pixels	pixels	0	12	-
t_8	HCCD period (4X binning)	ns	-	50	-
t_9	RST rising edge to CRLAST rising edge	ns	-	0	-
t_{10}	CR rise and fall time	ns	1	2	$0.25t_5$
t_{line}	Line readout time[3]	μs	-	443	-
t_{frame}	Frame readout time[3]	ms	-	927	-

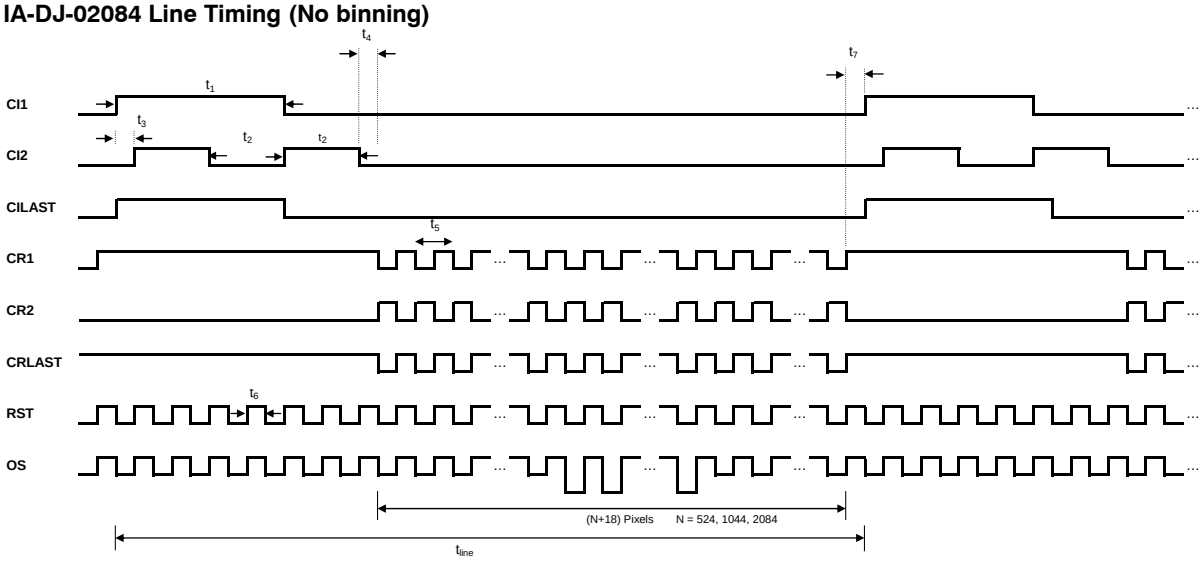
Notes:
1. fDATA = 5 MHz operation.
2. Full Width Half Maximum.

Line and Frame Readout Times

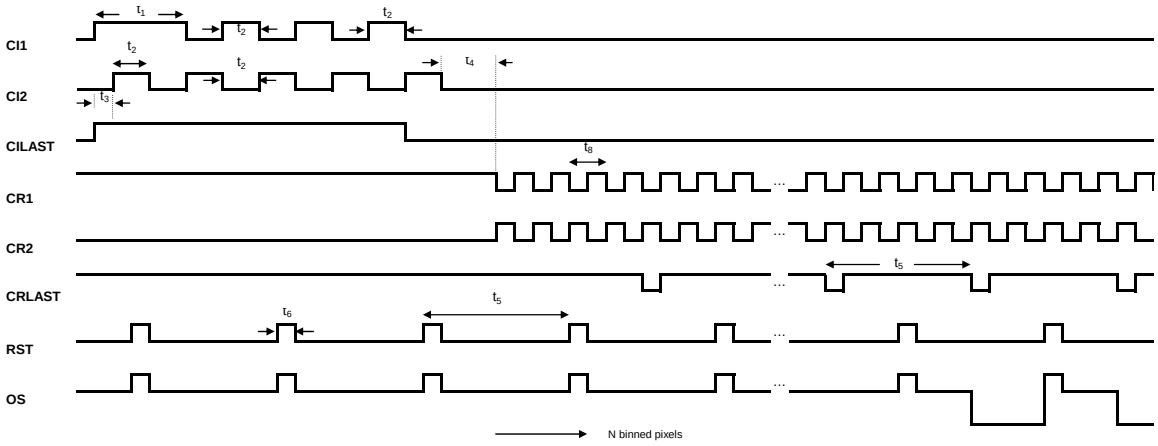
Symbol	Description	IA-DJ-00524	IA-DJ-01044	IA-DJ-02084
t_{line}	Line readout time[1]	133 µs	237 µs	445 µs
t_{frame}	Frame readout time[1]	71 ms	249 ms	931 ms

Note:
1. Max rate (no integration) with no binning

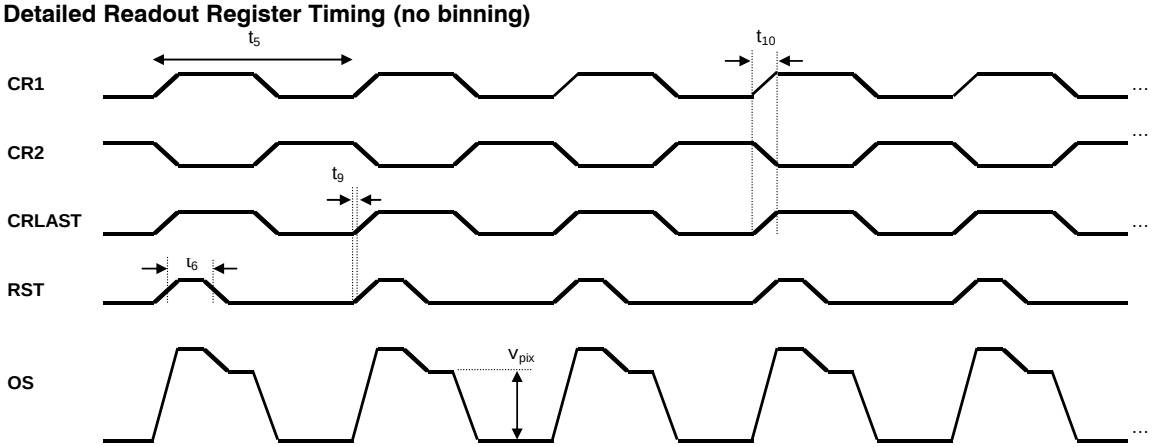
IA-DJ-02084 Line Timing (No binning)



Line Timing (4 × 4 binning)

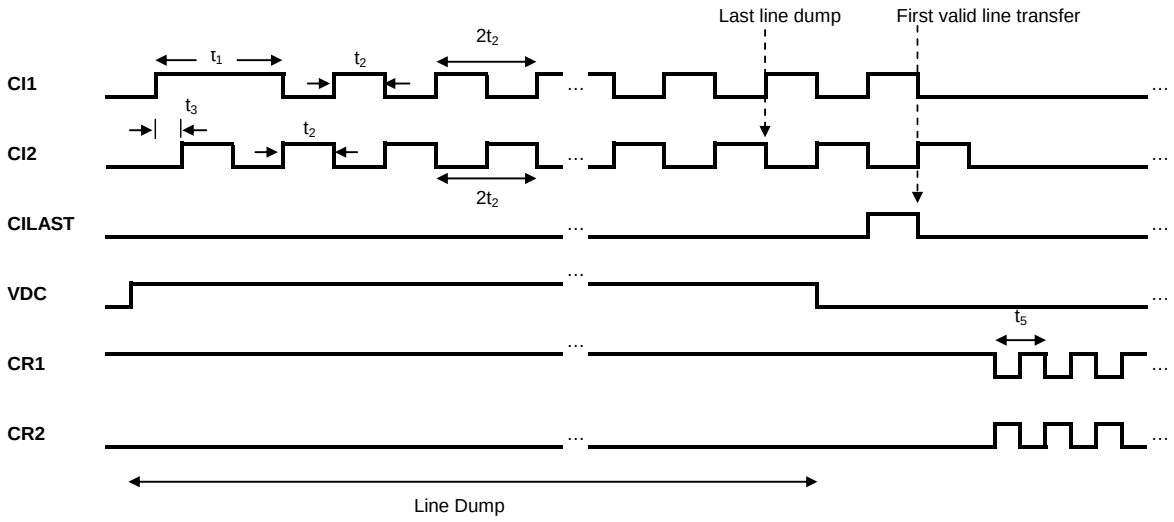


Detailed Readout Register Timing (no binning)



IA-DJ-02084 AOI Charge Dump

IA-DJ sensors have an AOI feature that allows charge dumping of unwanted lines into a charge drain until the desired line is reached. This allows for faster AOI readout. The charge dumping can be initiated by clocking the VDC gate.



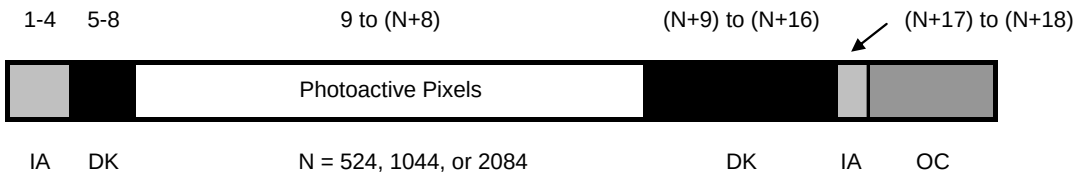
*NOTE: CRs can be clocked during charge dumping to reduce accumulated dark signal on HCCD.

AOI Sample Frame Rate Calculation (For IA-DJ-02084)

	1 × 1 binning		4 × 4 binning	
AOI Size	524 × 524	1024 × 1024	524 × 524	1024 × 1024
Frame Rate (fps)	4.0	2.1	27.6	19.7

Notes:
1. Power dissipation will increase during AOI charge dumping
2. N = AOI window size (N × N)
3. B = Binning (1, 2, 4)
4. Frame Read Time = $(t_1 + 2t_2\,(2084 - N + 4)/B) + (t_1 + 2t_2)\,(N + 4) / B + (2102)\,(N + 4)\,t_5 / B$
5. Frame Rate = 1 / (Frame Read Time)

IA-DJ Line Content



Notes:
1. IA: Inactive pixels
2. DK: Dark pixels
3. OC: Overclock pixels (user defined)

IA-DJ Image Sensor Flatness

	Units	Min.	Nominal	Max.
Die Flatness	μm Pk-Pk		25	TBD

Sensor Mechanicals

IA-DJ-00524

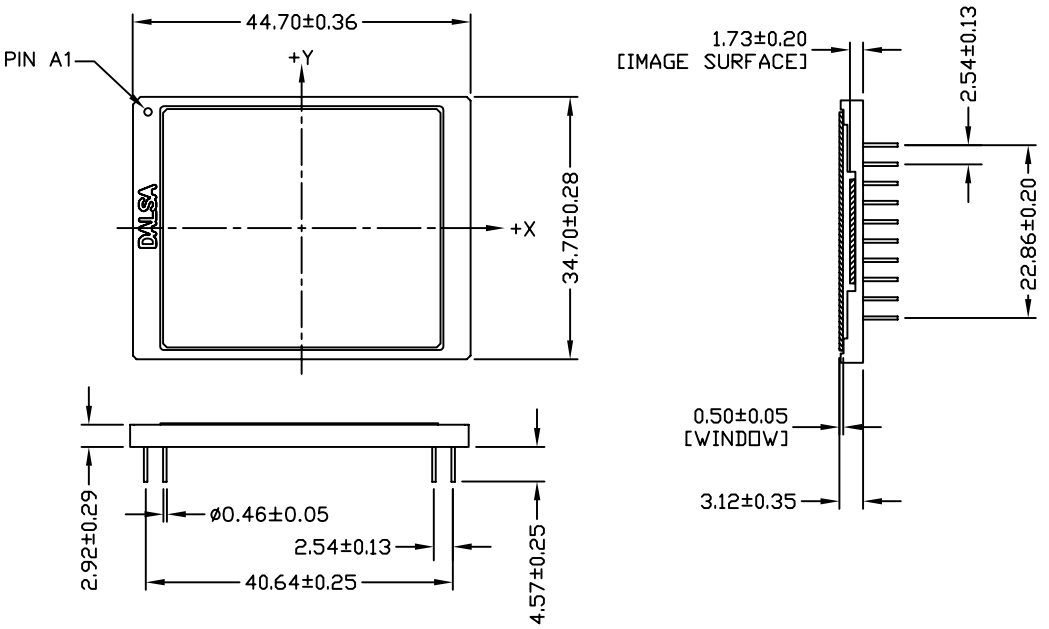


IMAGE AREA CENTER
WITH RESPECT TO
PACKAGE CENTER:
X = 0.00±0.25
Y = 0.00±0.25

UNITS: MM

IA-DJ-01044

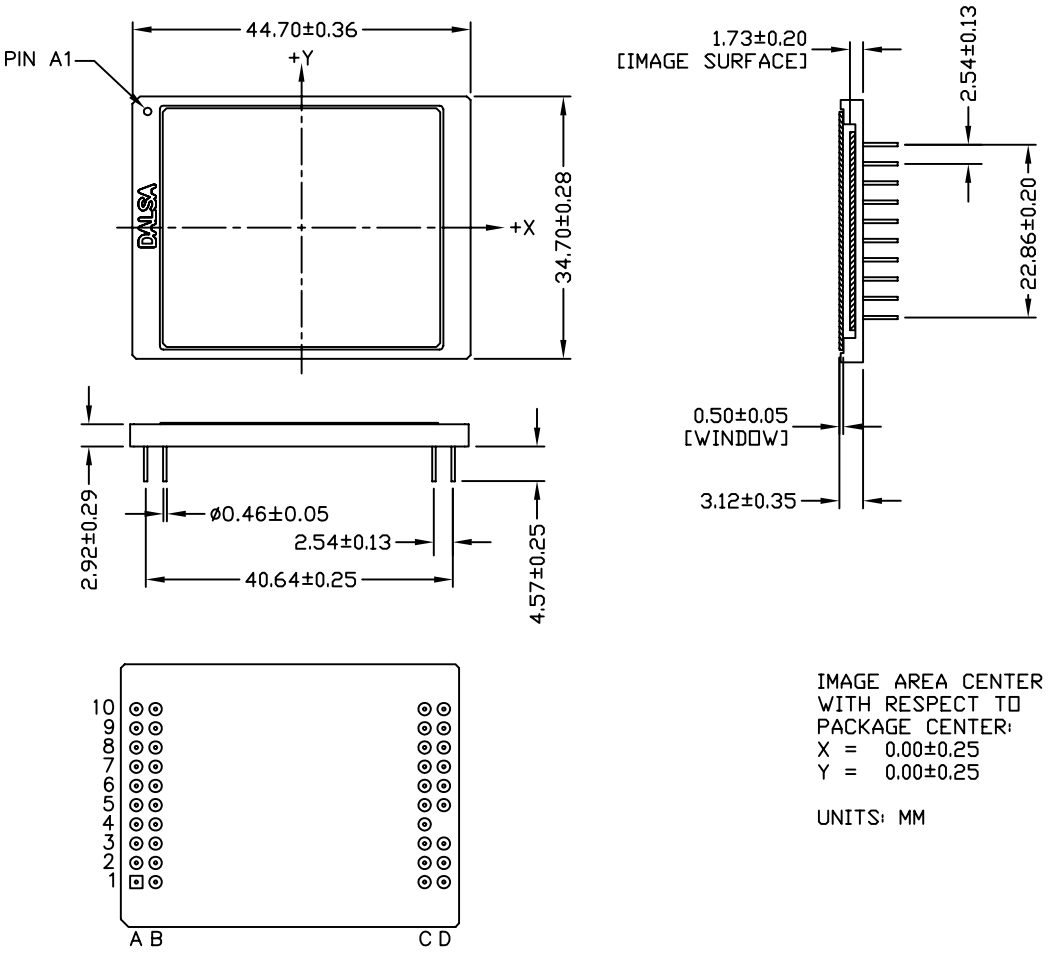


IMAGE AREA CENTER
WITH RESPECT TO
PACKAGE CENTER:
X = 0.00±0.25
Y = 0.00±0.25

UNITS: MM

A-DJ-02084 Package

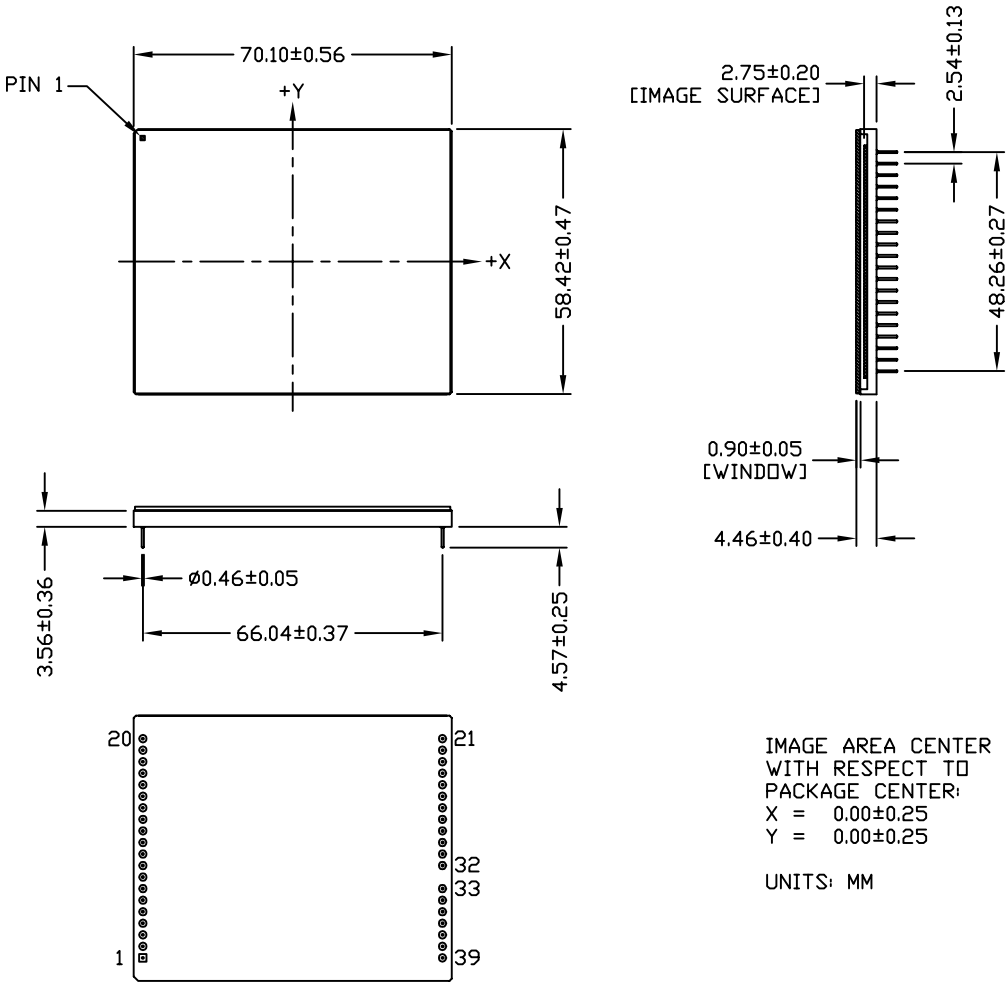


IMAGE AREA CENTER
WITH RESPECT TO
PACKAGE CENTER:
X = 0.00±0.25
Y = 0.00±0.25

UNITS: MM

IA-DJ Window Options

	IA-DJ-00524	IA-DJ-01044	IA-DJ-02084
Dimensions	31.5×36.7×0.5mm	31.5×36.7×0.5mm	69.5×58×0.9mm
AR Coating[1]	>98%, 400 to 700nm[2]	>98%, 400 to 700nm[2]	TBD

Notes:
1. AR coating both sides
2. At normal incidence

IA-DJ Ordering Information

Sensor	Cosmetic Grade	Window
IA-DJ-00524	Class I and Class II	Option 1: Permanently glued. Option 2: Temporary. Taped on.
IA-DJ-01044	Class I and Class II	Option 1: Permanently glued Option 2: Temporary. Taped on.
IA-DJ-02084	Class I and Class II	Option 1: Permanently glued Option 2: Temporary. Taped on.

Revision History

Number	Description	Date
00	Initial release.	February 11, 2009
01	-t9 timing parameters revised: min/max values removed and rec. values set to 0 ns. Page 10. -Cosmetic Spec table for IA-DJ-01044 revised to include Class II values, page 7.	September 3, 2009